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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,208	12/06/2005	Jose De Jesus Pineda De Gyvez	NL 030685	2758

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
01/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/559,208	PINEDA DE GYVEZ ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on ~~11/6/2005~~ 12/6/2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. As for claims 1 and 11, lines 7 and 9, and 5, and 11-13, respectively, applicant claims local control device (36) and local controllers (36). This is unclear because the claim language is used in both singular and in plural form, thereby rendering element the "local control device" as both singular and plural. Clarify.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Chandrakasan (US Patent Application 2004/0183588).

4. As for the claims, Chandrakasan discloses the invention as claimed, including:

1. An integrated circuit (40) comprising a plurality of computation islands (30), each computation island (30) operating at one or more utility values [paragraphs 0012, 0022-0023, 0043, 0047, wherein the device has a plurality of at least transistor pairs or "computation islands"], at least one utility value of a first computation island being different from a corresponding utility value of a second computation island [paragraphs 0023 and 0047], the integrated circuit (40) being provided with monitoring means (43) for monitoring at least one working parameter related to a working condition of the integrated circuit (40) [paragraphs 0070-0082 – controller "70"], and at least two computation islands being provided with a local control device (36) for independently tuning at least one utility value for at least one computation island, based on the monitored at least one working parameter [paragraphs 0070-0082, 0016, 0060, individual islands can be controlled. The claim language does not require physically different or separate controllers, however, at least the isolation wells "122" may be considered different than the controller "70". Further, controller "70" (paragraph 0074) may consist of one or more integrated circuits, thereby reading as global and local controllers], wherein the local control devices (36) are provided with communication means to communicate with a global controller (42) so as to obtain a pre-set level of performance of the integrated circuit (40) [paragraphs 0070-0082, 0015-0016, 0060. Further, controller "70" (paragraph 0074) may consist of one or more integrated circuits, thereby reading as global and local controllers];
2. An integrated circuit (40) according to claim 1, wherein the one or more utility values comprise one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck) [paragraphs 0012, 0022-0023, 0043, 0047];

3. An integrated circuit (40) according to claim 2, wherein the transistor threshold voltage is determined by a bulk voltage of some transistors in a computational island (30) [paragraphs 0045-0046, substrate bias voltage];

4. An integrated circuit (40) according to claim 1, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, clock frequency value [paragraphs 0018, 0070, 0079-0082, 0087];

5. An integrated circuit (40) according to claim 1, wherein the pre-set level of performance relates to any or all of power consumption or speed of the integrated circuit (40) [paragraphs 0011, 0043, 0047, 0053-0054].

6. An integrated circuit (40) according to claim 1, wherein each computation island (30) is placed in an isolated third well of a triple-well CMOS technology [paragraphs 0016, 0022-0023, 0060];

7. An integrated circuit (40) according to claim 1, furthermore comprising at least one interface island (39) for interfacing among computation islands (30) [paragraphs 0016, 0022-0023, 0060];

8. An integrated circuit (40) according to claim 7, wherein at least two interface islands (39) are placed in a common third well, or substrate, of a triple-well CMOS technology [paragraphs 0016, 0022-0023, 0060];

9. An integrated circuit (40) according to claim 1, a computation island (30) furthermore comprising an actuator (34) for tuning a utility value in a monitored utility value-regulating closed-loop system [paragraphs 0015-0016, 0022-0023, 0050-0058, 0060];

10. An integrated circuit (40) according to claim 1, a computation island (30) furthermore comprising a local monitoring means (38) for monitoring local working parameters of the computation island (30) [paragraphs 0070-0082, 0015-0016, 0060, individual islands can be controlled. The claim language does not require physically different or separate controllers, however, at least the isolation wells "122" may be considered different than the controller "70". Further, controller "70" (paragraph 0074) may consist of one or more integrated circuits, thereby reading as global and local controllers];

11. A method for real-time tuning of at least one utility value of an integrated circuit (40) comprising a plurality of computation islands (30) [see as cited in the rejection of claim 1];

each computation island (30) operating at one or more utility values [see as cited in the rejection of claim 1], at least one utility value of a first computation island being different from a corresponding utility value of a second computation island [see as cited in the rejection of claim 1], at least two computation islands being provided with a local control device (36) for independently tuning at least one utility value for at least one computation island (30) [see as cited in the rejection of claim 1];

the method comprising monitoring of at least one working parameter related to a working condition of the integrated circuit (40), based on the monitored at least one working parameter [see as cited in the rejection of claim 1], independently tuning at least one utility value for at least one computation island (30) by means of its local controller (36) [see as cited in the rejection of claim 1], and controlling the local controllers (36) of the computation islands (30) by means of a global controller (42) so as to obtain a pre-set level of performance oft he integrated circuit (40) [see as cited in the rejection of claim 1];

12. A method according to claim 11, wherein the one or more utility values comprise one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck) [see as cited in the rejection of claim 2];

13. A method according to claim 11, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, clock frequency value [see as cited in the rejection of claim 4];

14. A method according to claim 11, wherein the pre-set level of performance relates to any or all of power consumption or speed of the integrated circuit (40) [see as cited in the rejection of claim 5];

15. A method according to claim 11, wherein the integrated circuit (40) is designed based on utility values different from their nominal values [see as cited in the rejection of claim 2, and paragraphs 0050-0051, 0070-0082].

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/
Primary Examiner
Art Unit 2825

SAW
December 21, 2007